AN-222

Application Note

THE ABC's OF DC TO AC INVERTERS

Prepared by
Merrill Palmer
Applications Engineering

The author provides an exhaustive examination of the entire field of dc to ac inverters. Among the topics discussed are; the proper inverter for a specific application; operating principles of different types of inverters; the problem of proper device selection in the design of inverters, an inverter design example; and many more.

MOTOROLA Semiconductor Products Inc.

INTRODUCTION

Transistor dc to ac inverters are useful in a wide variety of applications. They power the complicated electronic systems of orbiting satellites and cool astronaut's suits. They are widely used to operate gyros and other airborne instruments. They provide ac power to operate the electric shaver in your car. Inverters may become increasingly important and widely used with the further development of economic low-voltage dc power sources such as solar cells, nuclear cells, fuel cells, etc.

It should be noted that rectification of the inverter output results in dc to dc conversion. Transistor inverters as described herein are, therefore, the "heart" of transistor dc to dc converters. However, when used as a converter, to provide rectified output the frequency and waveshape of the transistor circuit are unimportant, except as they relate to the efficiency and smoothing of the rectified output.

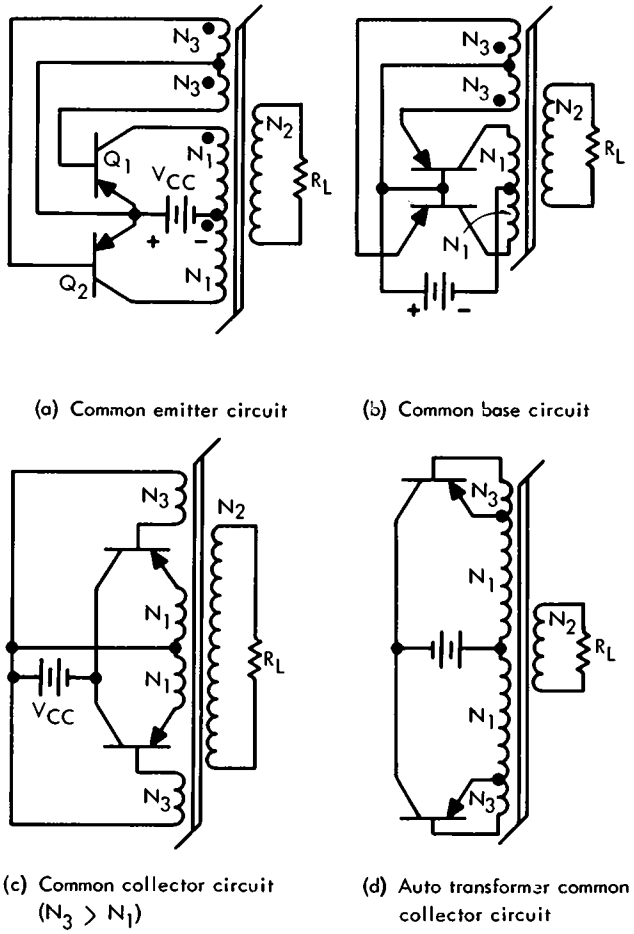


FIGURE 1 — BASIC ONE-TRANSFORMER INVERTER CIRCUITS

ONE-TRANSFORMER INVERTER OPERATION

Operational theory common to most transistor inverters may be illustrated by considering the basic over-driven, push-pull, transformer-coupled transistor oscillator circuit of Figure 1a, and the transformer B-H curve of Figure 2. Assume that transistor Q_1 is nonconducting, Q_2 conducting, and the transformer saturated at point J on the B-H curve. When Q_1 starts to conduct, the voltage developed across the primary windings N_1 induces voltage in the feedback windings N_3 such as to rapidly drive Q_1 into saturation and turn

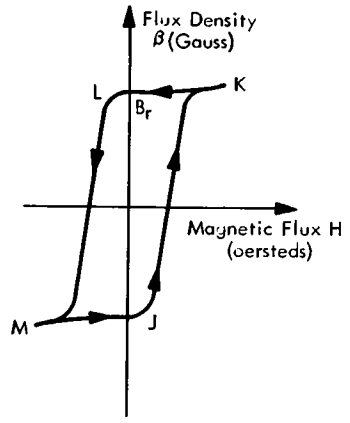


FIGURE 2 — TRANSFORMER B-H CURVE

Q_2 off. When this transition is completed, constant voltage $V_P = V_{CC} - V_{CE(sat)}$ is applied to N_1. Since $\frac{d\phi}{dt} = \frac{V_p}{N_1}$ flux ϕ must increase in the transformer core at a constant rate, causing flux density $B = \phi/A$ to increase from joint J toward point K on the B-H curve. As long as the core remains nonsaturated, magnetization current i_m ($=H/N_1$) is small, but as saturation (point K) is approached high magnetization current i_m is required to keep $\frac{d\phi}{dt}$ constant. When reflected load current, plus this sharply increasing magnetization current, exceeds the collector current which Q_1 can supply (with the drive available), Q_1 begins to come out of saturation causing V_p to decrease. V_{FB} and I_C decrease regeneratively, turning Q_1 off and ending the half cycle.

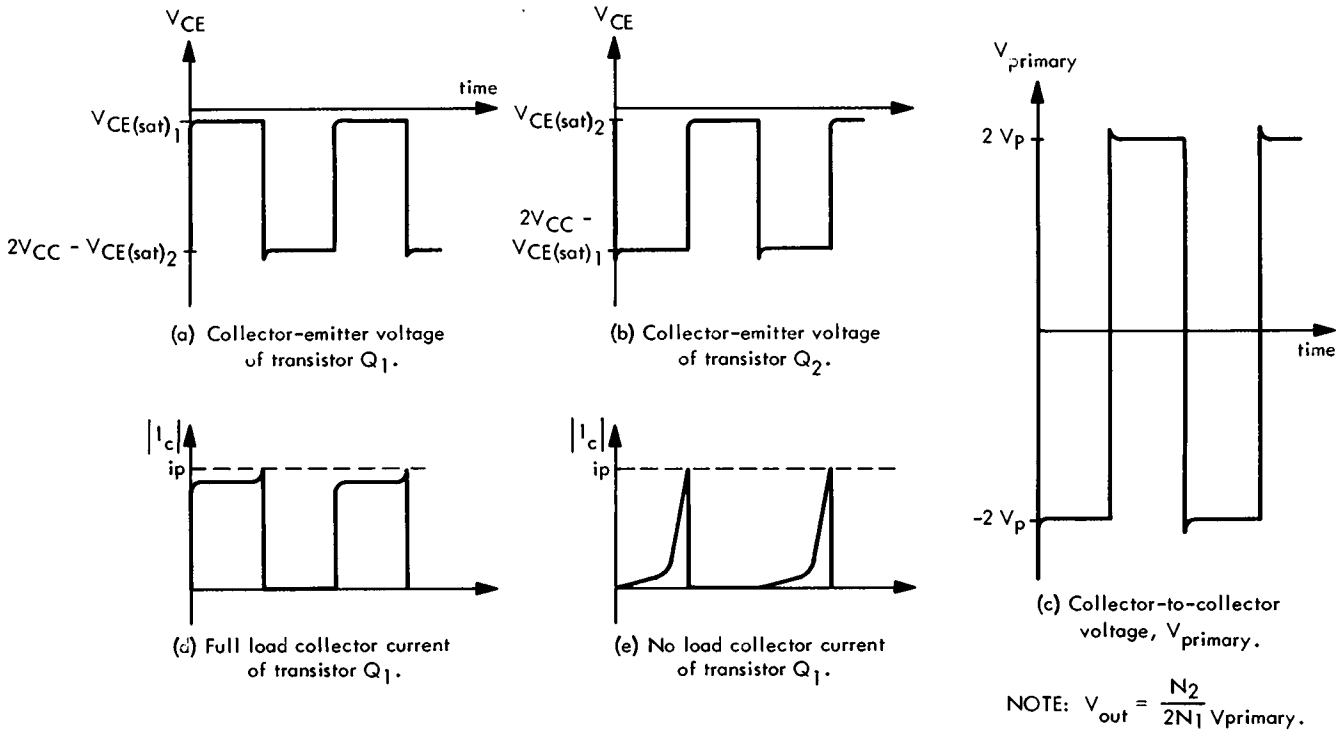
As flux in the transofrmer core collapses from point K to point B_r, voltage is induced in the winding which biases transistor Q_2 into conduction and initiates the next half cycle. The operation is similar to the first half cycle except that supply voltage (less $V_{CE(sat)}$) is applied to the other half of the primary, causing a reversal of polarity in the induced output-voltage. Q_2 conducts until the core is driven into negative saturation at point M on the B-H curve. As flux collapses from M to J the full cycle is completed.

Typical voltage and current waveforms for one transformer inverter operation are shown in Figure 3. It can be seen from the collector-to-emitter voltage waveforms that each device is subjected in the off condition to a voltage approximately twice the supply voltage plus any induced voltage that may occur in the circuit due to leakage inductance, etc. Also significant is the fact that the same maximum collector current i_p is required for switching action whether this current is primarily reflected load current, as in Figure 3d, or totally magnetization current, as in 3e. This will obviously limit efficiency at low output loads.

Operating frequency of the inverter is determined by the voltage V_p and by the saturation characteristics of the transformer core according to the relationship $f = \frac{V_p \times 10^8}{4\beta_s A N_1}$ cps. β_s is saturated flux density in gauss, A is cross-sectional area of the core in cm^2, and N_1 is the number of turns on one half of the primary.

TWO-TRANSFORMER INVERTERS

At high load currents high-frequency and high output-power the transformer requirements for the dual role



(a) Collector-emitter voltage of transistor Q_1.

(b) Collector-emitter voltage of transistor Q_2.

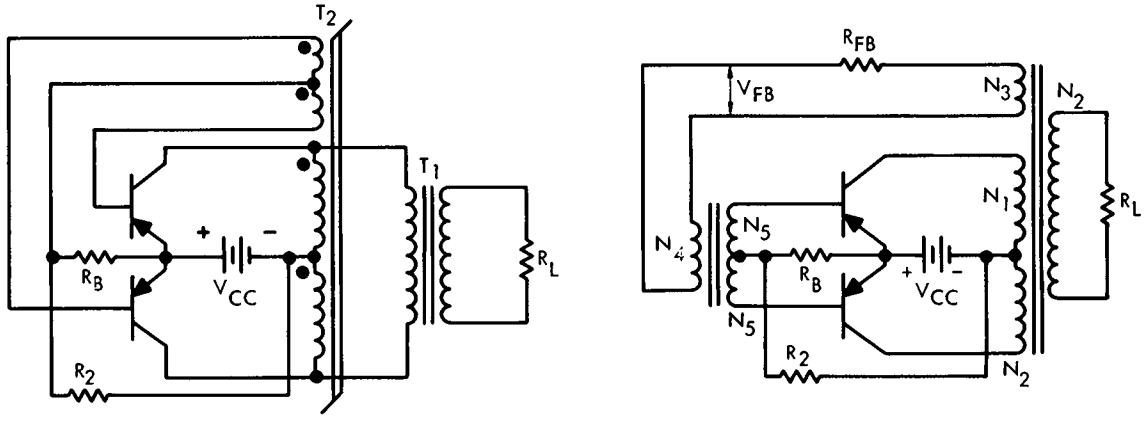
(c) Collector-to-collector voltage, $V_{primary}$.

(d) Full load collector current of transistor Q_1.

(e) No load collector current of transistor Q_1.

NOTE: $V_{out} = \frac{N_2}{2N_1} V_{primary}$.

FIGURE 3 — TYPICAL VOLTAGE AND CURRENT WAVEFORMS FOR ONE-TRANSFORMER INVERTER



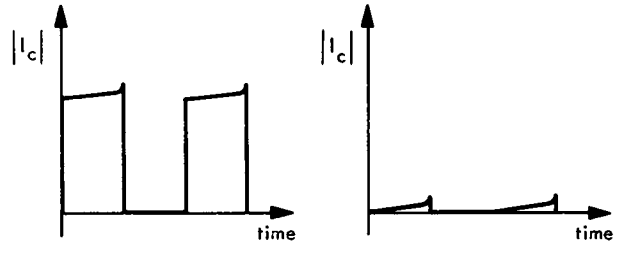
(a) Two transformer inverter with simple output transformer T_1.

(b) Two transformer inverter having easily regulated V_{FB}.

FIGURE 4 — TYPICAL TWO-TRANSFORMER INVERTER DESIGNS.

of frequency control and efficient transformation of output voltage become an increasingly difficult problem in one-transformer inverter design. For this reason, the two transformer inverter designs of Figure 4 are advantageous in many applications. Operation of two-transformer inverters is similar to the one transformer case except that in each circuit (Figure 4) only the small feedback transformer T_2 need be saturated. Since the magnetization current of T_2 is small, high current levels due to transformer saturation currents are reduced significantly compared to one-transformer design, as is device stress due to these transformer saturation current levels. (Compare Figure 5 with Figures 3d and 3e). Furthermore, use of a conventional output transformer with normal core material permits lower transformer costs as well as higher efficiency.

Another major advantage of two-transformer inverter design (a circuit such as Figure 4b) is that the inverter frequency is determined by V_{FB}. This voltage can fairly easily be regulated to provide constant frequency or can be changed with variable R_{FB} to provide variable frequency.



(a) Full load collector current

(b) No load collector current

FIGURE 5 — COLLECTOR CURRENT WAVEFORMS FOR TWO TRANSFORMER INVERTER.

ADDITIONAL TRANSISTOR INVERTER CIRCUITS

Single-transistor power-oscillator circuits are useful in low-power inverter applications in which their somewhat lower efficiency is of secondary importance when compared to the lower initial cost of the single transistor and a simple transformer. A typical basic one-transistor inverter circuit is shown in Figure 6. In the circuit of Figure 6 positive feedback, transformer saturation, and switching mechanism are similar to the two-transistor inverter, except that resetting action is caused by capacitor C rather than by a second transistor in push-pull configuration. Care must be taken to protect the device against excessive voltage "backswing" upon turn-off. For proper operation of this circuit, R_L and C must not overload the oscillator during the saturating half cycle, so that transistor conduction will be maintained until the transformer core saturates.

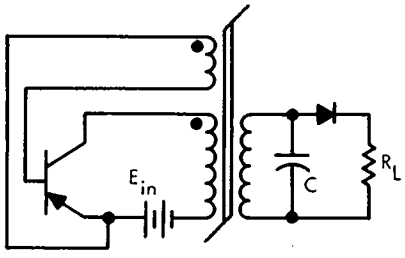


FIGURE 6 – BASIC ONE TRANSFORMER INVERTER CIRCUIT.

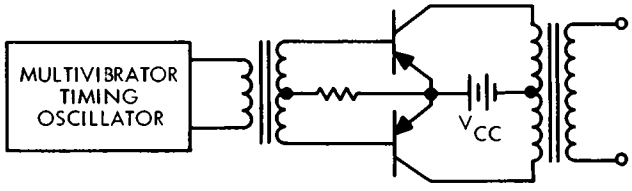


FIGURE 7 – TYPICAL DRIVEN INVERTER.

In driven inverters, such as shown in Figure 7, output-power-transistor switching is accomplished by multivibrator drive rather than by feedback from the output transformer. Multivibrator drive transistor inverters are useful for precision systems requiring carefully controlled frequency, waveform, etc., and for load independent systems. Load independent systems are especially attractive in the case of reactive loads, and when transient or starting conditions impose loads which would cause self-oscillating inverters to shut down or operate abnormally. Power requirements of the multivibrator are largely offset by nonsaturation of the output transformer and elimination of the feedback drive. The multivibrator driven inverter is not inherently less efficient than a self-oscillating inverter. However, use of the driven power stage as a linear amplifier rather than as a saturated switch will result in high dissipation in the transistors and low system efficiency.

Besides multivibrator drive, several other inverter circuits have been developed which do not use a saturating square loop transformer for switching action. These include the resistive-coupled transistor inverter, and inverters with such base circuit timing mechanisms as saturating base circuit inductors and the R-C timing and L-C tuned circuit timing familiar to basic oscillator theory.

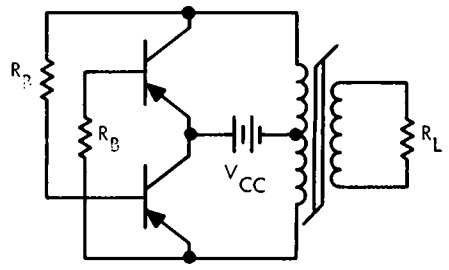


FIGURE 8 – RESISTIVE-COUPLED TRANSISTOR INVERTER.

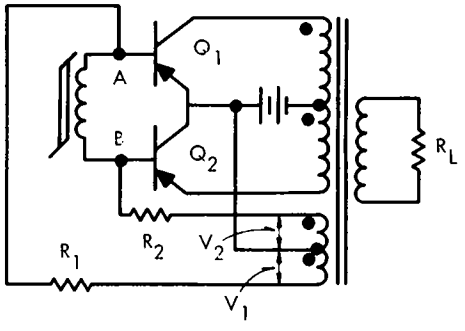


FIGURE 9 – SATURABLE BASE INDUCTOR TRANSISTOR INVERTER.

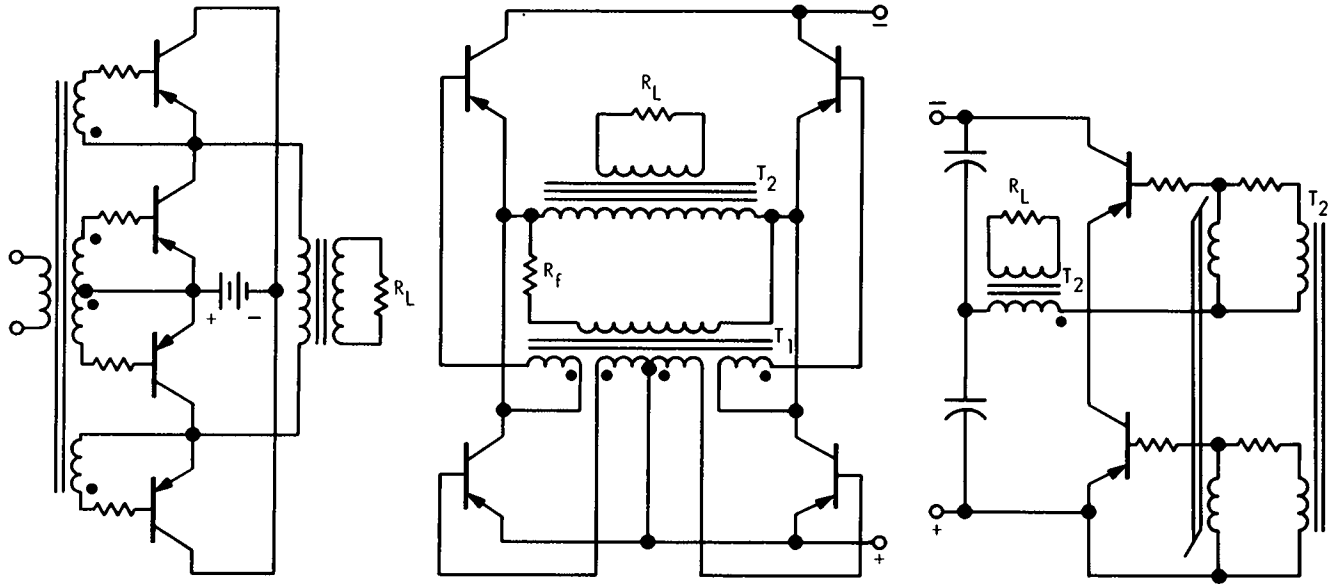
The resistive-coupled inverter of Figure 8 obtains the square wave drive from the transistor output by cross-coupled resistor feedback. This resistor coupled feedback oscillator is somewhat inefficient due to losses in R_B, and is difficult to control with regard to frequency.

An inverter design having saturable base inductor is shown in Figure 9. This circuit may be considered to be a simplication of the two-transformer inverter, except that the saturating transformer has been replaced by a saturable inductor connected between the bases of the two transistors. Switching occurs in the following manner: With transistor Q_1 is driven on by base current $i_B = \frac{V_1 - V_{BE}}{R_1}$ and Q_2 is biased off by V_2 through R_2. Voltage across the inductor is initially $V_{AB} = V_2 + V_{BE}$, but as the inductor saturates, V_{AB} collapses, essentially shorting out the feedback circuit. When this occurs, Q_1 loses its drive and turns off. The magnetization current of the transformer reverses the voltages, drives the system over in the opposite sense, and brings Q_2 toward conduction. As soon as the inductor comes out of saturation the positive feedback is effective and the second half cycle is begun.

Saturable base inductor design is simple, being largely determined by the following relationships: Letting $V_1 = V_2$ and $R_1 = R_2$, then $I_{B1} = I_{B2} = \frac{V_1 - V_{BE}}{R_1}$ and $f = \frac{(V_1 + V_{BE}) \times 10^8}{4 N A \beta_S}$ where N, A and β_S apply to the saturable inductor. The main drawback of this circuit is power loss in the base resistors.

BRIDGE INVERTERS AND SERIES CONNECTED INVERTERS

Inverters such as the bridge circuits of Figure 10, or the series connected inverter of Figure 11, are useful



(a) Driven bridge-connected output stage.

(b) Self-oscillating two transformer full bridge inverter.

(c) Half bridge inverter with saturable base inductors.

FIGURE 10 — TYPICAL BRIDGE INVERTER CIRCUITS.

when high-input supply-voltage exceeds transistor voltage capabilities. The bridge arrangements apply input supply-voltage across each off device, compared to approximately twice supply voltage in simple push-pull circuits. This reduction of voltage to which each device is subjected is true of all circuits of Figure 10, but in the half-bridge circuit of Figure 10c transistor current must double to maintain the original output-power.

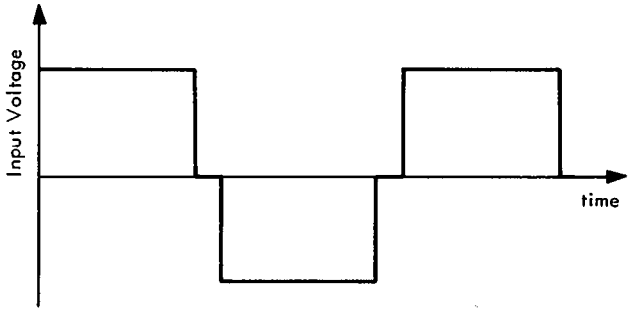


FIGURE 11 — TYPICAL MAGNETIC AMPLIFIER OUTPUT WAVEFORM USED AS BRIDGE INVERTER INPUT PREVENTS SIMULTANEOUS CONDUCTION OF BOTH INVERTER CIRCUIT HALVES DURING CONDUCTION.

In considering bridge inverters, the designer should be aware of a problem tolerable in simple inverters but of major significance in bridge connections. This has to do with the current-voltage excursions of the devices as the circuit switches. If the previously non-conducting side of the circuit turns on before the other side is essentially off, high voltage and high current may be imposed on the devices, and device safe-areas may be exceeded. Additionally, high transients may be generated. The problem may be somewhat alleviated by reducing device "on" drive, by device protection against transients, or by compensating base-drive networks which retard turn-on of the non-conducting device. One possibility is to use a driven bridge having the input waveforms of Figure 11.

In the circuit of Figure 12, n simple inverted connected in series divide the supply voltage equally so that each device is required to withstand $V_t \simeq \frac{2(V_{CC})}{n}$. The magnetic circuit requires that the voltage divide equally among the series stages.

Each of the basic approaches summarized above has a unique combination of advantages and disadvantages which should be considered in light of the design requirements.

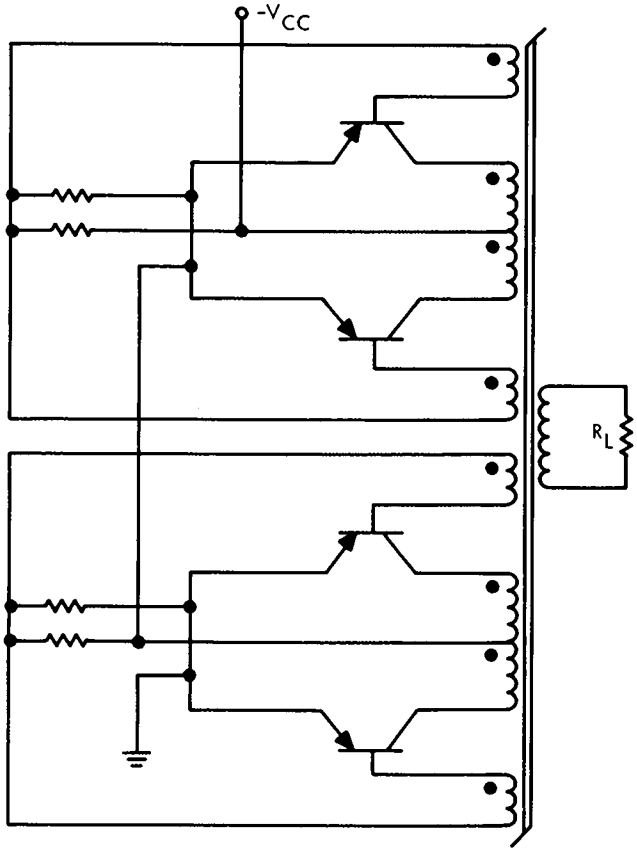


FIGURE 12 — SERIES CONNECTED INVERTERS FOR HIGH D-C INPUT VOLTAGES.

INVERTER SPECIFICATIONS

Some inverter characteristics which may be of importance to various applications are listed in Table I. It is the function of the inverter specifications to indicate which are important to the use intended, and to state via tolerances how critical each of these is expected to be. Obviously, the more characteristics simultaneously required and the tighter the tolerances, the more difficult and costly the design will be. In the absence of specifications requiring emphasis on other characteristics, inverters are usually designed for highest efficiency. Achievement of very precise frequency and output performance, etc. is usually at the expense of efficiency as well as circuit simplicity.

TABLE I — COMMONLY SPECIFIED INVERTER CHARACTERISTICS

Input voltage: range and nominal
Output power
Output voltage
Output frequency accuracy
Regulation of output voltage and frequency vs. load and input voltage
Load power factor
Output waveform
Harmonic distortion of output, if sinusoidal, vs. load, power factor, input voltage.
Overall efficiency vs. loading
Operating environments (temp., etc.)
Size and Weight
Protection required (as against shorted output, reversed polarity input, etc.)

INVERTER DESIGN FUNDAMENTALS

Discussion and sample design of a basic one-transformer inverter should serve to illustrate basic design fundamentals. Assume the following specifications are to be met: output power P_0 = 100 watts, $|V_{CC}|$ = 12.5 volts, V_{out} = 115 volts rms, 60 cps, into a resistive load.

The popular common-emitter circuit of Figure 1a was chosen for the example. The common-base circuit of Figure 1b is advantageous with low voltage input supplies, but the feedback windings must carry the high current of the emitter. Common-collector circuits permit direct collector to heat-sink mounting.

INVERTER TRANSISTOR SELECTION

Since much of inverter design is influenced by the performance characteristics of the transistor selected, it is desirable to make transistor choice at the outset. Transistor parameters important to inverter applications are summarized in Table II. Selector guides such as Figure 13, and manufacturers' semiconductor data manuals are helpful in making the transistor selection.[1]

The transistor type selected must be capable of maximum collector current $I_p = \frac{P_{in}}{V_{CC}} = \frac{P_o}{(V_{CC})\eta}$ where η is overall inverter efficiency. The transistor must have collector-emitter breakdown in excess of the "off" voltage, which is approximately twice supply voltage V_{CC}. Additionally, a margin of safety should be applied to allow for voltage transients from leakage inductance, transients of input voltage, etc. Device surge rating three times supply voltage is a reasonable rule of thumb. The transistor must have sufficient safe operating area that operating load lines are well within

TABLE II — INVERTER TRANSISTOR SELECTOR CRITERION

$I_{C(max)} > I_{C_P} = \frac{P_{out}}{\eta \cdot (V_{CC})}$
$BV_{CES} > V_{max} = 2\ V_{CC}$ + Circuit Transients $= 3\ V_{CC}$
Adequate safe operating area (as a preliminary choice assume I_p, 2.5 V_{CC}, 25 μ sec)
Low $V_{CE(sat)}$ at $I_C = I_{C_P}$
Adequate gain at $I_C = I_{C_P}$; (If possible, rapid fall-off of gain with increasing I_C above I_{C_P})
Fast switching response (high f_T)
$BV_{EBO} > V_{FB}$ or diode clamped E-B voltage
Low collector leakage at $V_{CE} = V_{max}$
Thermal adequacy:
Useful parameter values at operating junction temperature T_{J1}
$\theta_{jc} > \frac{T_{J1} - T_a}{P_{ave}} - (\theta_{chs} + \theta_{hsa})$ where T_a = ambient temp., θ_{chs} = case to heat sink thermal resistance, θ_{hsa} = heat sink to ambient thermal resistance
Cost
Size and weight
Availability
Adequate environmental capabilities (shock, temperature, moisture, etc.)

[1] See Motorola Semiconductor Data Manual, Section 6, "Power Transistors" 1965.

SELECTOR GUIDE

LOW FREQUENCY INVERTER TRANSISTORS (60-400 CPS)

POWER OUTPUT	TRANSISTOR VOLTAGE RATING (BVces)						
	30	45	60	75	90	120	160
50	2N3611	2N3612	2N3713*N 2N1541	2N3714*N 2N1542	2N3489*N 2N1543	2N2527	2N2528
100	2N1539	2N1540	2N3714*N 2N1541	2N3714*N 2N1542	2N3489*N 2N1543	2N2527	2N2528
200	2N1557	2N1558	2N3715*N 2N1546	2N3716*N 2N1547	2N3491*N 2N1543	2N2527	2N2528
500	MP504	2N2156	2N2153	2N2154	2N1548		

MEDIUM FREQUENCY INVERTER TRANSISTORS (400 CPS - 10 KC)

POWER OUTPUT	TRANSISTOR VOLTAGE RATING (BVces)							
	5	30	45	60	75	90	120	160
50	2N2912	2N3611	2N3612	2N3713*N 2N1551	2N3714*N 2N1552 2N2526	2N3489*N 2N2527	2N2527	2N2528
100	2N2528	2N2082	2N2081	2N3715*N 2N1551	2N3716*N 2N1552	2N3489*N 2N2527	2N2527	2N2728
200				2N3715*N 2N2832 2N2080	2N3716*N 2N2079 2N2080	2N3491*N 2N2527 2N2833	2N2527 2N2834	2N2528 2N2834
500					2N2079	2N2833	2N2834	2N2834

HIGH FREQUENCY INVERTER TRANSISTORS (10 KC - 50 KC)

POWER OUTPUT	TRANSISTOR VOLTAGE RATING (BVces)							
	5	30	45	60	75	90	120	160
50	2N2912	2N2832	2N3025* 2N2832	2N3026* 2N3713*N 2N3445*N 2N2832	2N3714*N 2N3446*N 2N2833	2N3489*N 2N2833	2N2834	2N2834
100				2N3715* 2N3447* 2N2832	2N3448*N 2N3716*N 2N2833	2N3492*N 2N2833	2N2834	2N2834
200					2N3716* 2N2833	2N3492*N 2N2833	2N2834	2N2834

NOTES: ALL TRANSISTORS ARE GERMANIUM PNP UNLESS OTHERWISE NOTED.

* INDICATES SILICON TRANSISTOR

N INDICATES NPN TRANSISTOR

FIGURE 13 – TYPICAL TRANSISTOR SELECTOR GUIDE.[3]

device capabilities.[2] As a preliminary selection criterion an operating point $I_C = I_p$, $V_{CE} = 2.5\ V_{CC}$, $t_p = 25$ μsec may be assumed.

Inverter transistor power losses limit overall inverter efficiency. Factors influencing these losses should be a transistor selection criterion. Transistor losses normally consist primarily of collector dissipation $i_c \cdot V_{CE}$ shown schematically in Figure 14. "On" dissipation $V_{CE\ (sat)} \cdot I_{C(on)}$ and "off" dissipation $V_P \cdot I_{CE}$ are usually low, and switching losses predominate, especially at high frequency. Switching load lines for inverter transistors and switching power losses are summarized in Figure 15. Inverter transistor efficiency is maximized by high h_{FE}, low $V_{CE(sat)}$, fast switching response, and low leakage in the off condition.

Additional transistor selection considerations include thermal adequacy, BV_{EBO} high enough to sustain feedback reverse bias or a clamped emitter-base reverse voltage, transistor size, weight, and cost. The choice between silicon or germanium transistors is essentially covered by the criterion above. In general, silicon transistor inverters are more temperature stable than germanium inverters and can be operated at higher temperatures, but silicon transistors are usually more expensive than germanium devices and have higher $V_{CE(sat)}$. Many silicon transistors have low BV_{EBO}.

The general groups of transistor characteristics desirable in inverter applications are not entirely compatible in practical transistors. High gain and low $V_{CE(sat)}$, fast switching response, high voltage, and extensive device safe area are compromised in device design. Each is achieved at some expense to the others, and emphasis of one or two parameter groups seriously detracts from the remaining groups. While

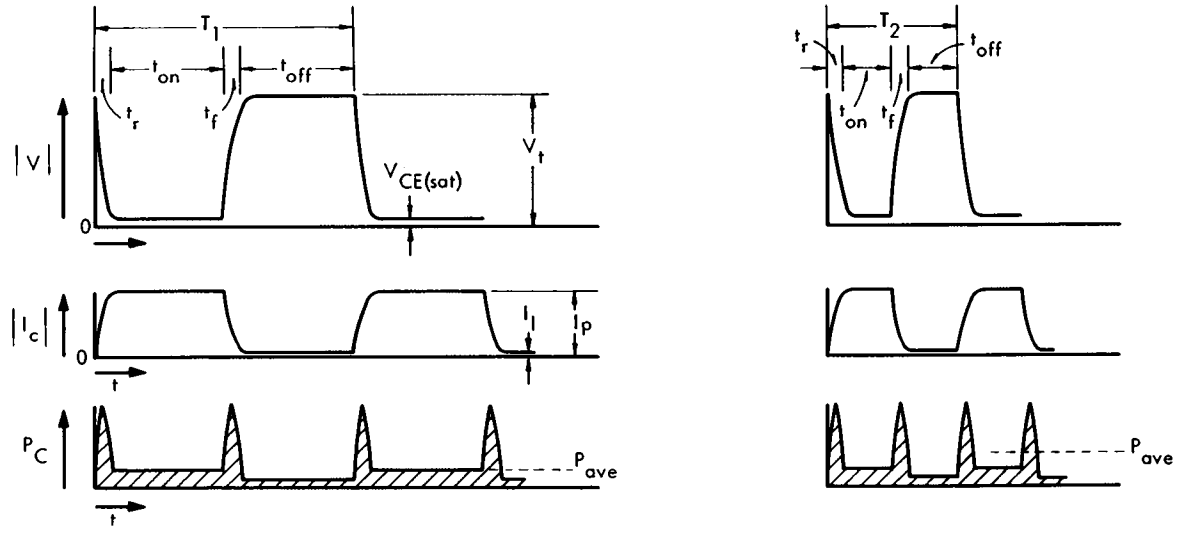


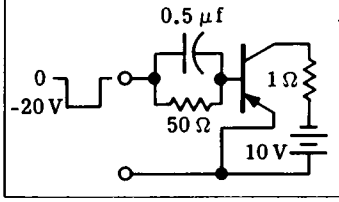
FIGURE 14 – TYPICAL INVERTER WAVEFORMS FOR I_C, V_{CE}, P_C(I_C V_{CE}) FOR TRANSISTORS OF D-C TO A-C INVERTERS.

[2] See Greenburg, Ralph "Determing Maximum Reliable Load Lines for Power Transistors." Application Note AN137-R1, Dept. TIC, Motorola Semiconductor Products Inc., Phoenix, Arizona.

[3] Motorola Semiconductor Data Manual, page 6-5, Motorola, Inc. Phoenix, Arizona, 1965.

TABLE III — IMPORTANT 2N1558 PARAMETERS PNP TO-3 GERMANIUM POWER TRANSISTORS

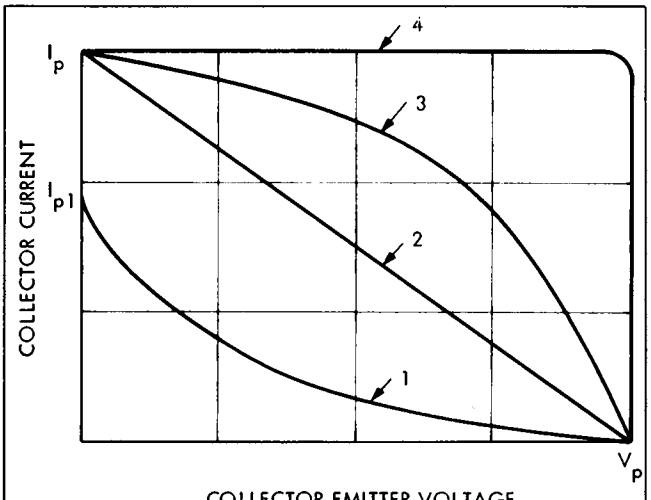
Maximum Continuous Collector Current:	15A
Collector Junction Temperature:	-65 to + 110°C
Thermal Resistance, ϕ_{JC}:	0.8°C/W max.
BV_{CES} (I_C = -300 mA)	45 volts min.
I_{CBO} (V_{CB} = -40 V)	3.0 mA max.
I_{EBO} (V_{EB} = -12 V)	0.5 mA max.
h_{FE} (I_C = -10 A, V_{CE} = -2 V)	50-100
V_{BE} (I_C = -10 A, I_C = -1 A)	0.7 V max.
$V_{CE(sat)}$ (I_C = -10 A, I_C = -1 A)	0.5 V max.
g_{FE} (I_C = -10A, V_{CE} = -2V)	12-40 mhos
Switching times in circuit below:	



$t_d + t_r$: 10 μsec typical

t_s: 5 μsec typical

t_f: 25 μsec typical



TYPICAL SWITCHING LOAD LINES FOR TRANSISTORS. SWITCHING LOSSES FOR THE ABOVE LOAD LINES ARE GIVEN BY THE FOLLOWING RELATIONSHIPS.

t_s = switching time (rise time or fall)

f = frequency

1. $P_1 = 2/9\ V_1 I_{p1} t_s f$ where peak power occurs @ $t_{s/3}$
2. $P_2 = 1/6\ V_p I_p t_s f$ where peak power occurs @ $t_{s/2}$
3. $P_3 = 2/9\ V_p I_p t_s f$ where peak power occurs @ $t_{s/3}$
4. $P_4 = V_p I_p t_s f$

FIGURE 15 — SUMMARY OF TRANSISTOR SWITCHING POWER LOSS.

this view is grossly oversimplified, it is useful to indicate that each transistor type available on the market represents one of many possible compromises between desirable parameters. The inverter designer must choose that compromise best suited to his particular application.

From the number of available power transistors which could have been chosen, 2N1558 was selected for the example under consideration. From the important inverter design parameters of 2N1558 summarized in Table III, it may be seen that this transistor type well satisfied the selection criterion discussed above, and is well specified at the anticipated operating current I_C = 10 A.[4]

Given output power P_o = 100 watts, let us assume an overall efficiency η, say 80%. Then input power $P_{in} = \frac{P_o}{\eta} = 125$ watts. Primary current $I_p = \frac{P_{in}}{V_{CC}} = 10.0$ A. 2N1558 h_{FE} (I_C = -10 A, V_{CE} = -2 V) is 50 to 100 so a minimum gain 2N1558 will require I_B = -200 mA for I_C = -10 A. However, additional base current is desirable to drive the transistor well into saturation, even as gain changes with temperature and transistor aging. Increased base current reduces $V_{CE(sat)}$ and transistor turn-on time, but increases base circuit dissipation and transistor turn-off time. The correct overdrive for optimum efficiency is therefore a rather complicated function which will have to be uniquely determined for each transistor type and operating current level. Forced gain of the circuit should usually be less than half of minimum device gain. Setting $\frac{I_p}{I_B} = \frac{h_{FE(min)}}{2}$ gives I_B = -400 mA.

It is noteworthy that maximum collector current upon transformer saturation is $I_B\ h_{FE}$. Magnetization current spikes will, therefore, be minimum if the transistor gain, h_{FE} falls off rapidly with increasing collector current above the operating current I_p. This characteristic is shown in Figure 16.

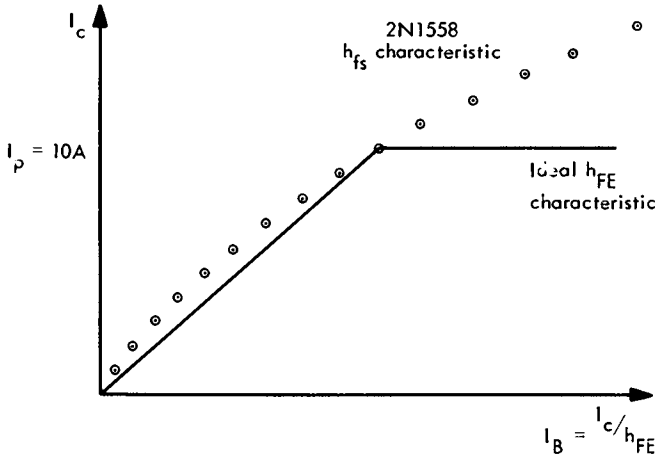


FIGURE 16 — COMPARISON OF 2N1558 I_c VS. I_b WITH IDEAL CHARACTERICTIC FOR INVERTER TRANSISTORS.

[4] For complete data including design curves and safe operating area, see Motorola Semiconductor Data Manual, Section 6 pp 52-55.

INVERTER TRANSFORMER DESIGN

Transformer design or selection is the next consideration. In a one-transformer inverter such as this example, the transformer determines frequency as well as output and feedback voltages. To accomplish this with acceptable transformer efficiency is the essence of the design problem.

From the transformer equation of page 3, inverter frequency $f = \frac{V_p \times 10^8}{4\beta_s AN_1}$ cps where effective cross-sectional area A of the core includes allowance for stacking factor of laminated or tape-wound cores. Given V_P and f, N_1 is determined by this equation as a function of core selection. $N_1 = \left(\frac{V_P \times 10^8}{4f}\right)\left(\frac{1}{\beta_s A}\right)$

Core selection is somewhat arbitrary, but must allow enough turns for good coupling and enough window area for the required windings. Additionally, core selection should provide minimal hysteresis and eddy-current losses.[5] For good efficiency, these core losses should be comparable in magnitude to resistive losses of the windings. Also influencing core choice are cost, size and weight of the overall transformer.

Tape wound toroids of 50-50 nickel-iron[6] are excellent cores for inverter applications. This material has high β_s, square hysteresis loop, low core loss, and is little effected by temperature over the useful temperature range of transistors. Toroids, properly wound, give very close coupling which is desirable in inverter transformers. C-cores and E, U, and I cores of good square loop material are also popular.

Once a tentative core selection has been made, $N_1 = \frac{V_p \times 10^8}{4\beta_s Af}$ $N_2 = \frac{k_1 V_o N_1}{V_p}$, and $N_3 = \frac{k_2 V_{FB} N_1}{N_1}$ where k_1 and k_2 are multipliers to compensate for transformer voltage drops and losses. $k_1 = k_2 = 1.05$ to 1.10 is a reasonable first assumption. In determining V_o for required output power, it should be noted that for a square wave $V_o = V_{peak} = |V|_{ave} = (V_{rms})(V_{FB})$ must be greater than transistor V_{EB} in the on condition, but must be less than BV_{EBO}, unless transistor reverse V_{BE} is clamped. With $V_{FB} \simeq V_{EB}$ the circuit performance is highly dependent upon transistor and temperature. High V_{FB} and a series base resistor $R_B = \frac{V_{FB} - V_{EB}}{I_B}$ reduces sensitivity to V_{EB}, and frequently improves transistor turn off - especially if a speed-up capacitor is used across R_B[7] - but losses in R_B are directly proportional to V_{FB}. For many power inverters V_{FB} on the order of 3 volts gives adequate base drive stability and control without exceeding reasonable dissipation losses.

The remainder of transformer design consists of determining adequate wire sizes for the windings, checking fit of the windings in available core window area[8] and determination of winding IR drop and I^2R losses, core losses, overall efficiency and voltage regulation. Transformer design procedure including detached instructions for these last named steps is well summarized in a number of electronic data handbooks.[9] Wire size is usually calculated on the basis of 700 to 1000 circular mils per amp.[10]

Duty cycle should be applied to peak winding current to obtain the average current for purposes of wire size calculation. For the example under consideration N_1, N_2, and N_3 carry currents of $I_C = 10$ A, $I_O = \frac{100 \text{ watts}}{115 \text{ volts}}$ and $I_B = 400$ mA respectively, with duty cycles of 50%, 100%, and 50%. On the basis of 1000 circular mils per amp, wire of N_1, N_2 and N_3 should be 5000, 870, and 200 circular mils minimum for the example. In calculation of total winding areas it must be recognized that there are two each N_1 and N_3 windings. For this example, wire area $A_w = 2N_1A_1 + N_2A_2 + 2N_3A_3$ where A_1, A_2, and A_3 are the respective cross-sectional areas of the wire in each winding, including insulation. Bifilar or trifilar windings are recommended for close coupling.

Transformer efficiency and voltage regulation may be determined from $\eta = \frac{(\text{watts out}) \times 100}{\left(\begin{smallmatrix}\text{watts}\\ \text{out}\end{smallmatrix}\right)+\left(\begin{smallmatrix}\text{core}\\ \text{losses}\end{smallmatrix}\right)+\left(\begin{smallmatrix}\text{copper}\\ \text{losses}\end{smallmatrix}\right)}$ and v. r. = $\frac{I_2\left[R_s + \left(\frac{N_2}{N_1}\right)^2 R_P\right]}{E_2} = \frac{\left[R_s + \left(\frac{N_2}{N_1}\right)^2 R_P\right]}{R_L}$ where R_p and R_s are resistances of primary and secondary windings.

Several design attempts may be needed to achieve a core and winding combination which will provide the required frequency and voltage relationships with acceptable efficiency. Finally, all assumptions made during the design must be checked, and adjusted if necessary.[11]

---

[5] Hysteresis loss (ideal): $P_h = fW_h \times 10^{-7}$ W/cm^3 where $W_h = \frac{1}{4\pi}\oint H d\beta$ ergs/cm^3 cycle for square loop material

Eddy current loss (ideal): $P_e = \frac{\pi^2 t^2 (\beta \max)^2 f^2}{\rho \times 10^{16}}$ W/cm^3 where t = thickness of individual flux carrier laminations

ρ = resistivity of the material.

[6] 50-50 nickel-iron is sold commercially as Orthonol, Deltamax and Hypernik V.

[7] Speed-up circuits are discussed on page 12.

[8] The ratio of wire area to available window area is the winding factor. Winding factor of 0.4 indicates good fit for a toroidal core. Higher "ideal" winding factors apply to cores having rectangular windows.

[9] For example, See I. T. T. Reference Data for Radio Engineer, Chap. 11 or Radiotron Designers' Handbook, Chap. 5.

[10] For current density as a function of output power, see I. T. T. Reference Data for Radio Engineers, page 274.

[11] Commercial transformers for one-transformer inverters are available for a variety of standard V_{CC}, f, P_o and V_o combinations. See Saladin, Power Inverter Circuits Using Off-the-shelf Components. Application Note AN134, Motorola Semiconductor Products Inc., Dept. TIC.

With the addition of R_B to the feedback circuits, the basic design is completed. However, two additional considerations which should receive design attention are starting circuits and speed-up circuits. In the interest of simplicity these topics were not previously discussed since they are not essential to basic theory of operation, but they are necessary in practical inverters.

TABLE IV — TRANSFORMER DESIGN FOR ONE-TRANSFORMER INVERTERS

Is a transformer commercially available which will do the job?

Core material should have square hysteresis loop, high β_s, low losses.

$$N_1 = \frac{V_p \times 10^8}{4 \beta_s A f} \qquad N_2 = k_1 \frac{V_o}{V_p} N_1$$

$$N_3 = K_2 \frac{V_{FB}}{V_p} N_1$$

Windings should have 100 to 1000 circular mils per amp.

$$\frac{\text{Wire area}}{\text{Window area}} \approx \text{0.4 for toroids, 0.7 to 0.8 for rectangular windows}$$

Core losses $\approx I^2R$ winding losses

$$\text{Efficiency } \eta = \frac{\text{Watts out} \times 100}{\text{Watts out} + \text{core losses} + \text{copper losses}}$$

Voltage regulation v.r. =

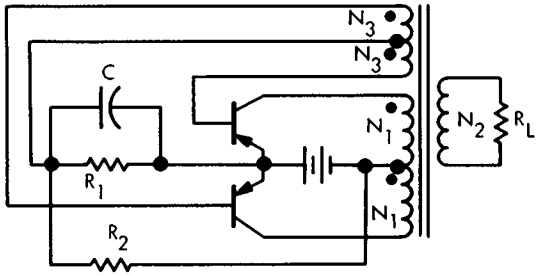
$$\frac{I_2 \left[R_2 + \left(\frac{N_2}{N_1}\right)^2 R_1\right]}{V_o} = \frac{\left[R_2 + \left(\frac{N_2}{N_1}\right)^2 R_1\right]}{R_L}$$

Use bifilar or trifilar windings for close coupling.

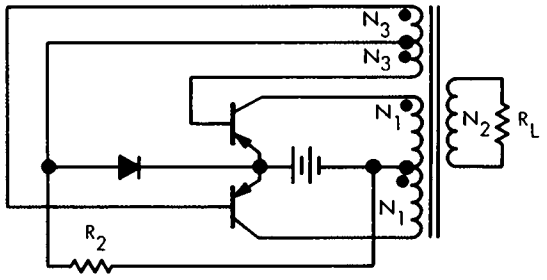
Check thermal aspects of transformer operation.

INVERTER STARTING CIRCUITS

In general, the basic circuits of Figure 1 and their derivatives including basic two-transformer inverters will not oscillate readily unless some means is provided to begin oscillation. This is especially true at full load and low temperature, the most severe starting requirement for resistive loads. The discussion of basic inverter operation assumed that one of the transistors was conducting — a condition resulting in oscillation. To assure this condition is the function of the starting circuit.

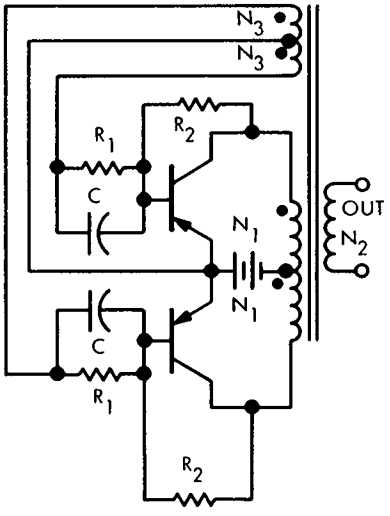


(a) Simple resistive self-starting circuit with speed-up capacitor across R_1.

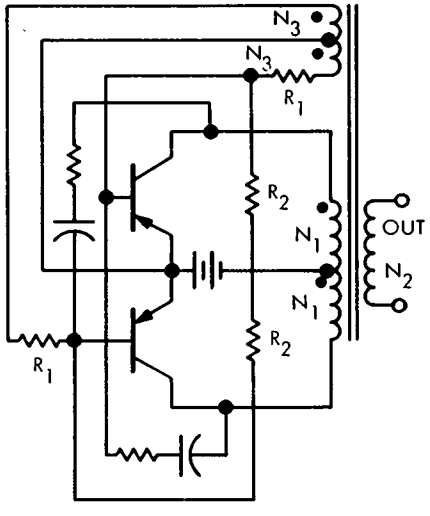


(b) Diode self-starting circuit.

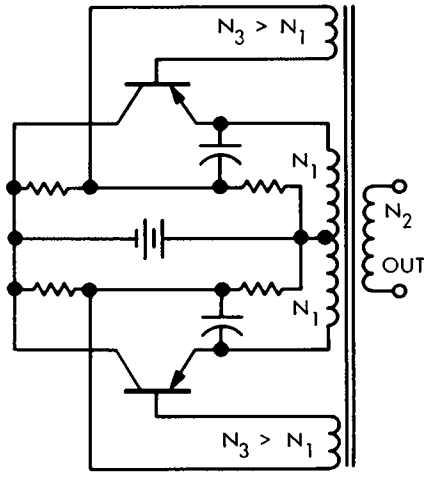
FIGURE 17 — STARTING CIRCUITS FOR TRANSISTOR INVERTERS.



(a) Basic common-emitter inverter circuit with individual starting and speed-up circuitry.



(b) Cross-coupled feedback capacitors as speed-up mechanism for common-emitter transistor inverter.



(c) Common-collector inverter with speed-up circuit.

FIGURE 18 — SPEED-UP CIRCUITS FOR TRANSISTOR INVERTERS.

A simple, commonly used starting circuit is shown schematically in Figure 17a. In this circuit R_1 and R_2 form a simple voltage divider to bias the transistors to conduction before oscillation starts. A good rule of thumb for the base starting bias developed by this circuit is to use 0.3 volts for germanium transistors and 0.5 volts for silicon. This voltage $V_B = \frac{R_1 V_{CC}}{R_1 + R_2}$. Since R_1 occurs in the feedback circuit in series with the base of each circuit half, R_1 must not exceed $R_B = \frac{V_{FB} - V_{EB}}{I_B}$. If R_1 is set equal to R_B, then R_1 and R_2 are uniquely determined for any given starting bias. The value of R_2 may be adjusted if starting characteristics are not satisfactory. This straight forward starting technique is advantageous in that only resistor components need be added to the circuit, but has the disadvantage of additional power dissipation, which may become excessive in high power circuits.

An improved but somewhat more costly starting circuit is shown in Figure 17b.[11] This circuit requires less dissipation than its resistance counterpart and is less temperature dependent. Operation is similar to the resistive case, but when power is first applied the bases of the transistors are driven negative by full supply voltage and oscillation starts rapidly.

Inverter loads such as capacitive filters, starting motors or incandescent lamps may temporarily present extremely high loads during the starting period. Starting requirements of such loads are often somewhat simplified by using a driven inverter, and this approach may be preferable to the circuit complications needed to assure self-oscillation.

INVERTER SPEED-UP CIRCUITS

Inverter speed-up circuits improve transistor switching and inverter efficiency. Improved switching is especially important at higher frequencies (See figure 14). A common speed-up method is to add a capacitor to the circuit. The circuits of Figure 18 usually produce improved switching waveforms.[12]

ADDITIONAL DESIGN CONSIDERATIONS

Finally, it must be determined whether circuit modifications are desirable and necessary to protect against inverter damage due to output overload or short circuit, input transients, input polarity reversal, etc. Shorted output causes cessation of inverter oscillation, but intermediate overload may cause transistor failure. Undesirable collector-emitter voltage spikes caused by input voltage transients or high transformer leakage inductance may be protected against by zener diodes connected collector-to-emitter. Despiking may also be accomplished by a series resistor and capacitor across the full primary winding or between collector and base of each transistor, but these arrangements slow transistor switching. If the transistors will not sustain reverse voltages resulting from input polarity reversal, protection may be provided by a diode in series with the input terminals. Since diode drop loss detracts from efficiency when the inverter operates properly, the lower dissipation circuit of Figure 19 may be preferable.

TABLE V — SUMMARY OF BASIC ONE-TRANSFORMER DESIGN

Given or assumed: P_o, V_{CC}, V_{out}, f

Design formula:

$P_{in} = \frac{P_{out}}{\eta}$ $\quad I_p = \frac{P_{in}}{V_{CC}}$

Transistor selection (Table II)

$I_B = \frac{I_p}{h_{FE(min)}}$ + overdrive $= \frac{2I_p}{h_{FE(min)}}$

Transformer design or selection (Table IV)

$f = \frac{V_p \times 10^8}{4\beta s A N_1}$ $\quad N_2 = \frac{k_1 V_o}{V_p} N_1$ $\quad N_3 = K_2 \frac{V_{FB}}{V_1} N_1$

$V_{EB} = V_{FB} \leq BV_{EBO}$ (use 3 + volts for V_{FB})

$R_B = \frac{V_{FB} - V_{EB}}{I_B}$

Starting circuit: For figure 16a $V_B = \frac{R_1 V_{CC}}{R_1 + R_2}$

(Recommended V_B: 0.3V for germanium, 0.5 V for silicon)

Speed-up Circuit

Operational Tests:

V_o, f, η, V.R. vs.	load	Starting
	V_{CC}	Waveforms (speed-up circuits)
	temp	Transistor operating temperature and load lines
		Transient operation.

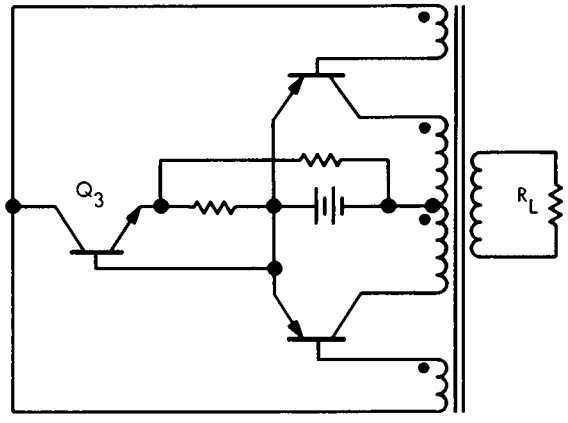


FIGURE 19 — REVERSE POLARITY PROTECTION WITH BASE CONTROL USING TRANSISTOR Q3.

[11] Roddam, Chapter 8 discusses some fifteen significantly different starting circuits, as well as common-collector circuit starting characteristics. See Bibliography.

[12] For additional speed-up circuits including speed-up transformer windings, see Lloyd.

When the inverter is constructed, its performance characteristics should be checked against the design. Thermal operation and transistor I_C vs. V_{CE} load lines should be checked, including load lines with maximum anticipated input transients.

Design procedures for the basic one-transformer transistor inverter are summarized in Table V.

Design of two-transformer transistor inverters requires procedure very similar to that of the one-transformer circuit, except that frequency is determined by primary voltage of the saturating drive transformer. The output transformer should oscillate at a frequency at least 10% lower than the inverter-frequency-determining drive transformer.

SINUSOIDAL OUTPUT INVERTERS

The basic inverters discussed heretofore have output frequency and voltage directly proportional to supply voltage. Output is square wave. For sinusoidal output, or for very tightly controlled frequency or output voltage regulation, the inverter must be modified from this basic circuit.

Sinusoidal output is required for gyro instruments and in some other applications. Obtaining undistorted sinusoidal output at high efficiency is difficult at best, and is further complicated at high power levels and low frequencies. Tuning and/or filtering the output of a basic inverter are straightforward approaches to realization of sinusoidal output. Practical circuits similar to those of Figures 20 and 21 have been used to achieve very low distortion sinusoidal outputs with efficiencies up to 80% at moderate power and fairly high frequencies.[13] Notice that inductor L_2 is added in series with the supply to isolate the supply and to absorb voltage swing of the primary due to the tuning or filtering. At extremely high supply currents, L_2 becomes bulky and expensive, and protective zener diodes between the collector-and-emitter of each transistor may be preferable to L_2.

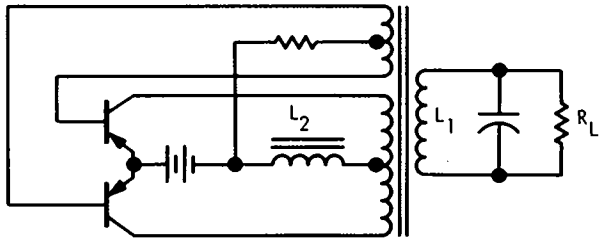


FIGURE 20 – TYPICAL TUNED OUTPUT OSCILLATOR CIRCUIT.

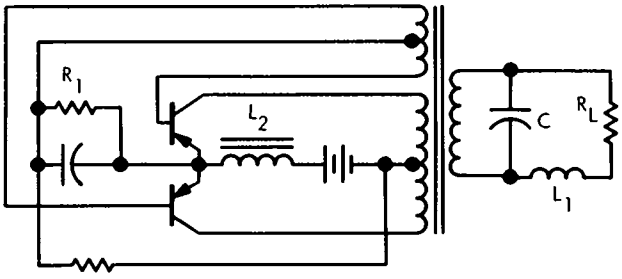


FIGURE 21 – FILTERED OUTPUT BASIC INVERTER.

For tuned circuits such as Figure 20 with high loaded Q of the tuned circuit and L_2 sufficiently high to provide essentially constant "on" current, the relatively high efficiency waveforms of Figure 22 are attainable. This has been referred to as Class D operation.[14] Self oscillating tuned Class C oscillators are another tuned output possibility.

For low power and/or high frequency, filtering is a good approach to attaining sinusoidal inverter output, but here again reactive component values become unwieldy, at high power and low frequency, and filter losses become significant. Conventional filter design applies, except that the converter may not operate properly if the filter input presents large inductive or capacitive loads. This is due to capacitive loading,

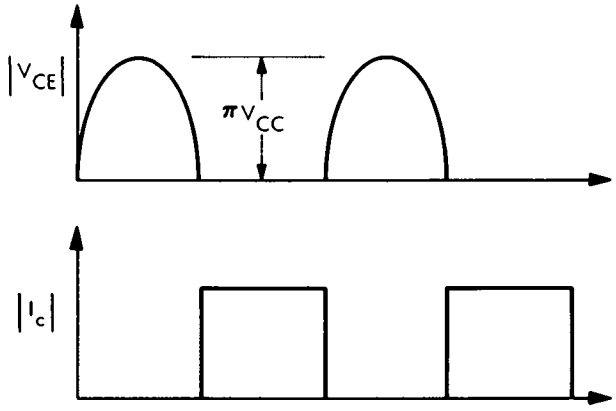


FIGURE 22 – TRANSISTOR WAVEFORMS OF "CLASS D" OPERATION CLAIMED BY BAXANDALL FOR OSCILLATOR OF FIGURE 21.[15]

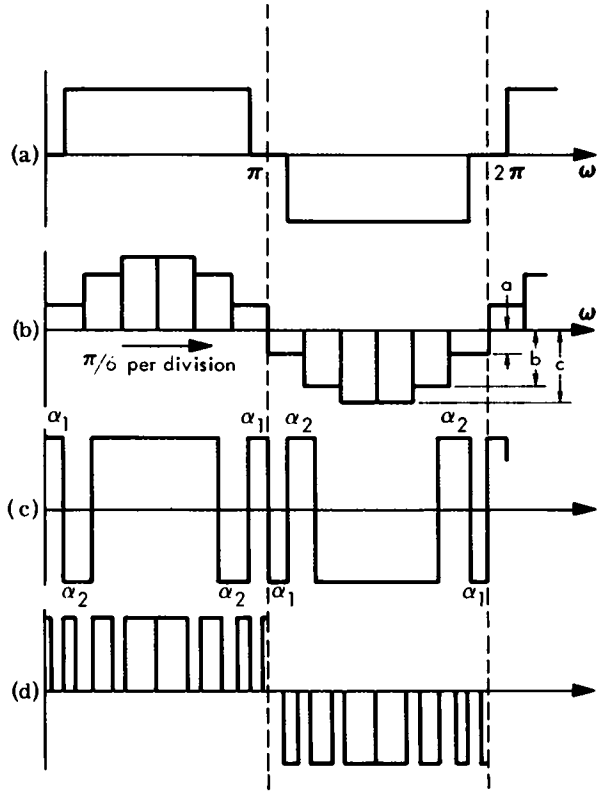


FIGURE 23 – SINUSOIDAL INVERTER PRE-FILTERED OUTPUT WAVEFORMS OF REDUCED HARMONIC CONTENT.

[13] See Baxandall: "Transistor Sine Wave LC Oscillators" Proceedings I. E. E. 106B pp 748-758 (1959).

[14] See Baxandall: Ibid, pp 751-752. Baxandall also discusses a "Voltage Switching Oscillator" which provided excellent 1.4W sinusoidal output at 45 kc with 85% efficiency.

[15] Baxandall: Ibid, pp 754.

or to inductive voltages reflected back into the primary. For good filtering, the series output inductor of Figure 21 or of a constant k or m-derived filter will probably be sufficiently high, that unless series tuning at the fundamental frequency is employed its reactive voltage drop will be appreciable. Transformer secondary voltage and current must be designed adequate to offset voltage drops and loading affects of the output filter.

At frequency and power such that only limited efficiency is achieved with tuned or filtered output or where reactive component size, weight or costs are prohibitive, the 78.5% theoretical maximum stage efficiency of a Class B driven sinusoidal output becomes reasonably attractive.[16] This is especially true if load independence, and the frequency stability, and control of the driven inverter are advantageous. The master-oscillator driven power-amplifier approach is common in precision frequency sinusoidal inverters.

Among the more sophisticated approaches to high efficiency sinusoidal inverter power are stepped waves, notched waveforms, and high-frequency pulse-modulation, all followed by filtering of greatly reduced requirements. The stepped waves of Figure 23a and 23b have no harmonics below the fifth and eleventh, respectively. These stepped waveforms are perhaps most efficiently realized by parallel inverters which are phase related,[17] or which are master control triggered.[18] The notched waveform of Figure 23c can be used to nullify all third and fifth harmonics at some increase in higher, more easily filtered harmonics.[19] A driven output in switching mode is an efficient means of achieving such a notched system. Modulation techniques such as the pulse-width modulation circuit of Figure 23d and Figure 24 have been used to achieve good efficiency at high power and low frequency with low size and weight.[20] These more sophisticated systems may readily be seen to achieve their advantages only at the cost of circuit complication and are probably justifiable only if sinusoidal output is absolutely necessary and a simpler approach is inadequate.

PRECISION FREQUENCY INVERTERS

Tape recorders, phonographs, clocks, etc. are among the few applications which require reasonably close inverter frequency control. Frequency accuracy of about 5% may be achieved by adding regulation to the feedback circuit. Regulating feedback transformer primary voltage in the two transformer inverter is fairly simple. For better frequency accuracy a separate frequency source is usually used to synchronize or drive the basic inverter.[21] Another possible approach is to control frequency by external voltage or controlled feedback voltage using multiple core transformers.[22] This technique also may be used to obtain variable frequency, and offers several advantages as a voltage to frequency converter.

INVERTER VOLTAGE REGULATION

Inverter output voltage regulation is improved by regulation of the input supply voltage and low output impedance design, but for very good output regulation over a wide range of loading output regulation circuitry may be necessary. Series pass regulation of input voltage is a popular approach. Pulse width modulation and magnetic amplifier control of the output are also promising regulation techniques for inverters.

MULTIPHASE INVERTERS

Systems of combined single inverters offer advantage in some applications. Inverter systems are frequently used to obtain 2-phase and 3-phase output.

A typical 3-phase inverter is the oscillator and amplifier of Figure 25. The 3-phase oscillations are supplied by an oscillator R-C coupled so that 120° phase difference exists at the collectors of the 2N651 transistors. An emitter-follower amplifier drives the output power transistors. The power transistors are operated in saturated switching mode.

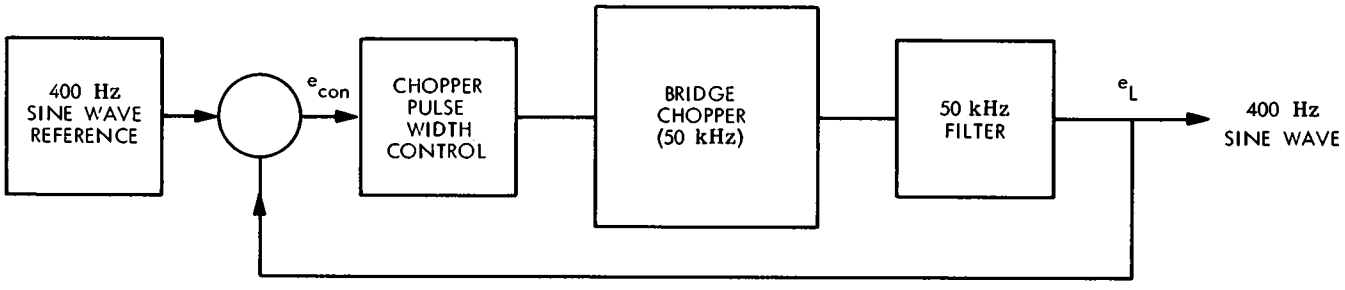


FIGURE 24 – BLOCK DRIVE OF BRIDGE CHOPPER INVERTER.

[16] Filtering requirements are greatly reduced when sinusoidal output replaces square wave output.

[17] Rodamm 205-220

[18] Salters, "A High Power D.C.-A.C. Inverter with Sinusoidal Output" diags. Electronic Engineering 33: 586-91 Sept., 1961. Describes system for generation of Figure 24b waveforms using SCR inverters.

[19] Turnbull, "Selected Harmonic Reduction on Static DC-AC Inverters" diags IEEE Transactions on Communications and Electronics 83: 374-8 July 1964.

[20] Morgan, "Bridge Chopper Inverter for 400 cps Sine Wave Power" IEEE Transactions on Aerospace Volume 2 Number 2 April 1964 993-997 describes a bridge chopper inverter which uses pulse width modulation to achieve 85% efficiency at 100 watts sinusoidal output.

[21] Braham "Satic Inverter Design Considerations" diags. Electronics 35:59-60 Ocyober 26, 1962.

[22] Sterling, et al "Multiple Cores Used to Simulate a Variable Volt-Second Saturable Transformer for Application in Self-Oscillating Inverters" IEEE Transactions on Communications and Electronics 83:288-94 May 1964.

An alternative 3-phase inverter approach uses Hartley oscillator driven flip-flops to supply control signal for the three phases in proper rotation, while still another practical circuit consists of a master push-pull stage and two phase-related driven stages.[23] A three-legged autotransformer may be incorporated in the output to provide exact 120° phase spacing if the three voltages are equal. Extreme unbalance of phase load may necessitate feedback control. It is to be noted that some inverters may be used for one-phase and 3-phase loads simultaneously providing the capacity of the phase also carrying the single phase load is not exceeded.

23 Roddam 205-216

CONCLUSIONS

Transistor inverters provide many advantages in conversion of d.c. power to a.c. The basic two-transistor, one-transformer design has excellent efficiency and performance, but at power in excess of 100 watts or if precise frequency is required, the two-transformer design is advantageous. Design requirements are dictated by inverter specifications, and modifications to the basic circuit probably will be necessary to achieve sinusoidal output or precisely controlled frequency or output voltage. For very complex requirements, inverter systems may be advantageous.

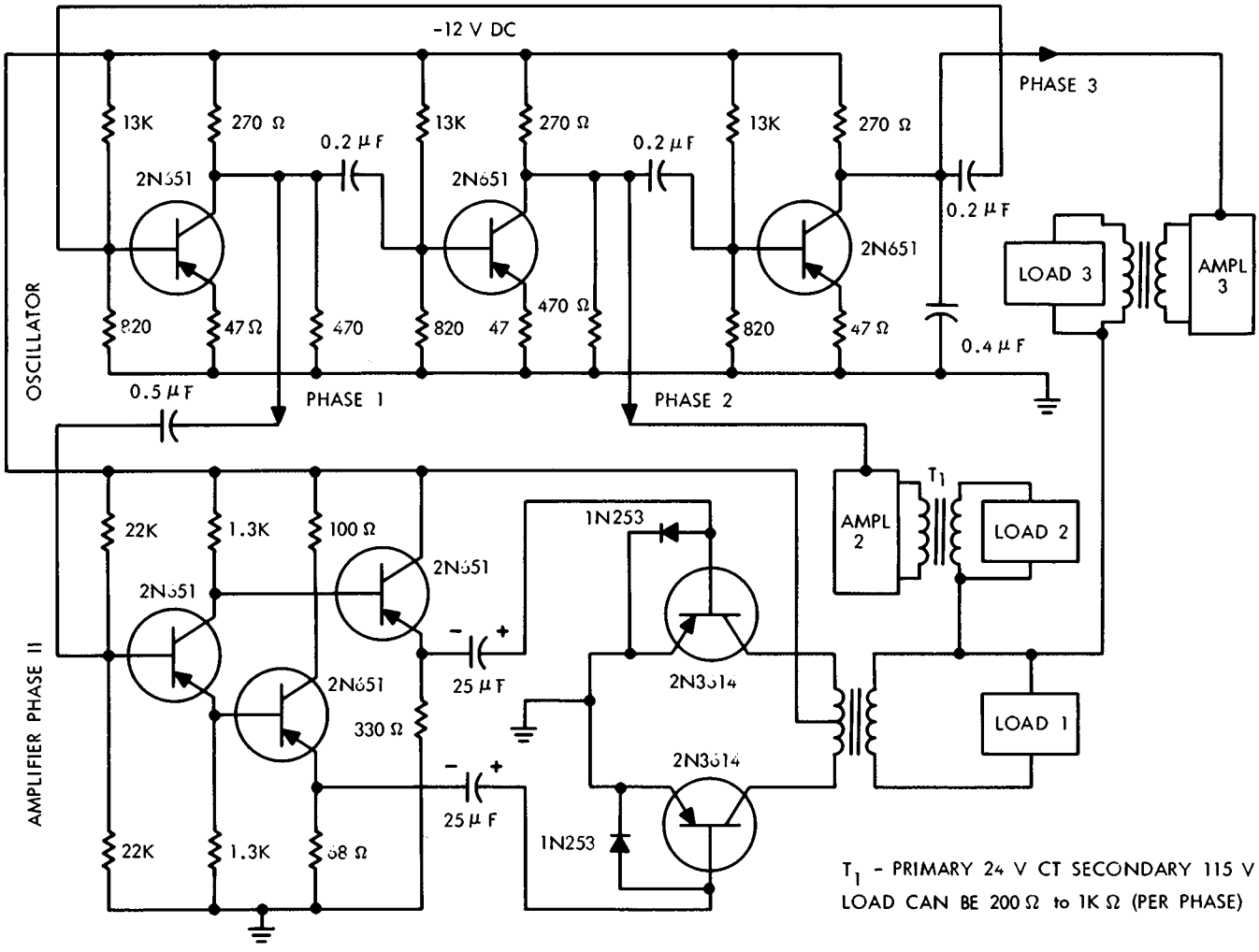


FIGURE 25 — 20 WATT 3-PHASE INVERTER, 12-VOLT D-C TO 115-VOLT 400 Hz A-C.

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